of figure 1(b), and respectfully submits that the Examiner is incorrect and should reconsider and withdrawn the objection to claim 1.

The features of dependent claims 2 and 11 objected to by the Examiner is the use of "a material with a high melting point that prevents unwanted metallurgical changes". Applicant respectfully submits that the specification at page 13, line 20 teaches that the melting point of the conductive metal "should be sufficiently high to prevent melting or other unwanted metallurgical changes during further processing of the silicon" and does so in the same language as used in the claims. This portion of the specification is a general section not discussing a particular embodiment, but relevant to all embodiments. This section discusses "processes to form the exemplary structures of the first section of the detailed description", and thus includes the specific embodiment of figure 1(b), which is the first section of the detailed description starting at page 4. Applicant respectfully submits that the "unwanted metallurgical changes" found at page 13, line 20 is sufficient to shown that there clearly is support in the specification for the recited features of dependent claims 2 and 11, and requests that the Examiner reconsider and withdrawn the objection to claims 2 and 11.

The Examiner states on page 2, eighth line that "a metal comprises one of tungsten and a tungsten alloy" is not found in the specification. Applicant respectfully disagrees and submits that the use of tungsten is found on page 2, line 18 in the summary of the invention section, which relates to the selected embodiment of figure 1(b), and at least at page 10, line 11 in the section dealing with general processes for all of the embodiments of the first section of the detailed description. Applicant respectfully submits that clear support exists in the specification for the recited features of dependent claims 4 and 18, and requests that the Examiner reconsider and withdrawn the objection to claims 4 and 18.

The Examiner states on page 2, line that "a second depth being greater than the first depth" is not found in the specification with regard to the embodiment of figure 1(b). Applicant respectfully disagrees and submits that in the section discussing figure 1(b) it states that it "might have an additional level of buried elements", which being an additional level is at a different depth from the first level. The second level may be deeper than the first level, or it may alternatively be shallower than the first level. The objected to feature of claims 8 and 15 is thus easily found in the very portion of the specification directly referring to the embodiment of

figure 1(b), and is also found in those portions of the specification that refer to all of the embodiments. In view of the above, Applicant respectfully requests that the Examiner reconsider and withdrawn the objection to claims 8 and 15.

The Examiner states on page 2, fourteenth line that a buried layer "substantially parallel to the active semiconductor layer" is not found in the specification with reference to claim 9. Applicant respectfully disagrees and submits that, as noted above the section of the specification related to the embodiment of figure 1(b) does refer to more than a single layer of buried elements, and the figure shows the elements 112 and 114 as being parallel to the active semiconductor layer 118, as discussed in the specification at least at page 5, line 29. The other objected to features of claim 9 have been discussed above with reference to the objection to claim 8. In view of the above, Applicant respectfully requests that the Examiner reconsider and withdrawn the objection to claim 9.

The Examiner states on page 2, fifth from last line that "conductive parts that extend upwardly on opposite sides of the first buried layer beyond the first depth" is not found in the specification with relation to claims 12 and 20 and the embodiment of figure 1(b). Applicant respectfully disagrees and submits that, as noted above, the section of the specification related to the embodiment of figure 1(b) does refer to more than a single layer of buried elements, and the portions of the specification that generally relate to all the embodiments discloses that the two or more conductive element planes may have "a three-dimensional semiconductor structure", as found in the summary of the invention section on page 2, lines. A three-dimensional semiconductor structure is believed to include vertical conductive structure from the lower conductive element plane and thus meet the features of claims 12 and 20. However, in the interest of furthering the allowance of the present subject matter, Applicant has cancelled claims 12 and 20 without prejudice, and reserves the right to reintroduce those claims.

The Examiner states on page 2, second from last line, that "conductive elements located either in front of or behind the deep trench capacitor" is not found in the specification with respect to claim 15. Applicant respectfully disagrees and submits that in the very section of the specification referring to the embodiment of figure 1(b) on page 6, line 5, it states that the "additional level of buried elements" might be "located either in front of and/or behind the plane of the trench capacitor". Thus essentially the same wording as found in claim 15 is found in the

specification in the section discussing the selected embodiment of figure 1(b), and therefore the Examiner is incorrect in suggesting that support for claim 15 is missing. Applicant respectfully requests that the Examiner reconsider and withdrawn the objection to claim 15.

The Examiner states on page 2, last line to page 3, fourth line that "active device layer includes ... (DRAM) ...(SRAM) ... (SDRAM) ... (EDO RAM) ...(BEDO RAM) ..." is not found in the specification.. Applicant respectfully disagrees and submits that the summary of the invention section relates to all embodiments and discusses general memory devices at page 2, line 25. The fourth part of the detailed description section, which section relates to all embodiments, at page 4, line 2 states that "a representative memory device" is presented. On page 14, line 27 states that it "will be appreciated by those skilled in the art, the present invention is not limited to any particular type of memory device", and thus the embodiment of figure 1(b) may include any type of memory device in the claims and find support in the specification such that one of ordinary skill may read and understand that the embodiment the recited memory types, which specifically include on page 14, line 29 to page 15, memories such as DRAMs, SRAMs, flash memory, SDRAMs, EDO RAMs, and BEDO RAMs, precisely as found in the claim 16, and even in the same order as found in claim 16. Thus essentially the same wording as found in claim 16 is found in the specification in the section discussing all of the embodiments, and therefore the Examiner is incorrect in suggesting that support for claim 15 is missing. Applicant respectfully requests that the Examiner reconsider and withdrawn the objection to claim 16.

Drawings Objection

Applicant respectfully submits that the drawings do provide enablement commensurate with the scope of Claims 1-2, 4, 8-9, 11-12, 15-16, 19-21 for the following reasons, as was discussed in detail in the previous response dated 5 January, 2005, which is incorporated herein by reference, and respectfully requests that the objection be withdrawn.

The Examiner states on page 3, that "substantially parallel buried conductive elements" is not found in the figures as recited in claim 1. Applicant respectfully disagrees and submits that figure 1(b) shows two buried conductive elements 112 and 114, which are shown parallel to each other and going into the page, as discussed on page 5 of the specification. Applicant respectfully

requests that the Examiner reconsider and withdrawn the objection to the drawings with regard to claim 1.

The Examiner states on page 3, that "a material with a high melting point" is not found in the figures as recited in claims 2 and 11. Applicant respectfully disagrees and submits that in the section of the specification that refers to all of the embodiments on page 8, it discloses in figure 3(c) that the layer 308 is formed of tungsten, a material that is well known in the art to have a high melting point. Applicant respectfully requests that the Examiner reconsider and withdrawn the objection to the drawings with regard to claims 2 and 11, and claims 4 and 18 as well.

The Examiner states on page 3, that "conductive elements oriented in a second direction, a second depth being greater than the first depth, and a deep trench capacitor" is not found in the figures with respect to claims 8 and 15. Applicant respectfully disagrees and submits that figure 1(b) clearly shows the deep trench capacitor 120, and that the specification section that refers to all of the embodiments, on page 8 discloses in figure 3(e) that there are conductive elements having two different depths, with one depth being greater than the second depth. Applicant respectfully requests that the Examiner reconsider and withdrawn the objection to the drawings with regard to claims 8 and 15.

The Examiner states on page 3, that "buried layer being substantially parallel to the active semiconductor layer" with respect to claim 9 is not found in the figures. Applicant respectfully disagrees and submits that figure 1(b) and the specification at page 5 shows that the conductor elements 112 and 114 are going into the page and are thus parallel to the plane of the active layer 118. The specification at page 6, line 4 points out that there may be an "additional level of buried elements", which would also be parallel to the active layer 118. Applicant respectfully requests that the Examiner reconsider and withdrawn the objection to the drawings with regard to claim 9.

Claims 12 and 20 have been cancelled without prejudice herein. Applicant respectfully requests that the Examiner withdrawn the objection to the drawings with regard to cancelled claims 12 and 20.

The Examiner states on page 4, that "parallel second conductive elements are located either in front of or behind the deep trench capacitor" is not in the drawings with respect to claim 15. Applicant respectfully disagrees and submits that figure 1(b) shows the deep trench

capacitor, and that on page 6, line 5, it states that the "additional level of buried elements" might be "located either in front of and/or behind the plane of the trench capacitor". Applicant respectfully requests that the Examiner reconsider and withdrawn the objection to the drawings with regard to claim 15.

The Examiner states on page 4, that "the active device layer includes" DRAMs and other types of memory, is not in the shown in the drawings with respect to claim 16. Applicant respectfully disagrees and submits that active area 118 in figure 1(b) and the specification at least at page 14, line 29 to page 15, shows that the layer 118 may be formed into various memories such as DRAMs, SRAMs, flash memory, SDRAMs, EDO RAMs, and BEDO RAMs. Applicant respectfully requests that the Examiner reconsider and withdrawn the objection to the drawings with regard to claim 16.

The Examiner states on page 4, that the "metal comprises on of a non-radioactive element, with regard to claim 19, and "a second direction orthogonal to the first direction, with regard to claim 21 are not found in the drawings. Applicant respectfully disagrees and submits that figure 1(b) shows the metal 112 and 114, the specification at page 5, in the section discussing the embodiment of figure 1(b), states that there may be a second level of conductive elements, which second level of conductive elements is not necessarily parallel to the first and thus may fairly be held to be orthogonal in an embodiment, as would be clear to one of ordinary skill in the art. The specification in the section related to all embodiments on page 14 discloses that the conductive elements, such as 112 and 114 of figure 1(b), may be formed from non-radioactive elements as found in the claims. Applicant respectfully requests that the Examiner reconsider and withdrawn the objection to the drawings with regard to claims 19 and 21.

Thus the drawings are shown to be proper under 37 CFR 1.83(a), no new drawings should be required, and the objection should be withdrawn.

§112 Rejection of the Claims

Claims 1-21 were rejected under 35 USC § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the

invention, as was discussed in detail in the previous response dated 5 January, 2005, which is incorporated herein by reference.

The Examiner states on page 5 that the specification provides not support for a plurality of "parallel buried conductive elements" as per claim 1. Applicant respectfully disagrees and submits that figure 1(b) does show more than one buried conductive element (112 and 114), that they are surrounded by an insulating material (116), that they are separated from the active layer (118), and that there is a capacitor (120) between the conductive elements. All of the elements of claim 1 are found in the selected embodiment of figure 1(b) and discussed in the specification at least in the section related to figure 1(b) at page 5. This was clearly discussed in the previous response and the Examiner has not refuted any of Applicant arguments. The Examiner has merely restated that "there is no support in the elected embodiment of figure 1(b) for the claimed limitations, as recited in claims 1-21", with no example or objective evidence of any kind provided. In light of the above, Applicant respectfully requests that the Examiner reconsider and withdrawn this rejection.

The Examiner states on page 6 that the specification does not provide support for claims 8 and 15, with regard to the embodiment of figure 1(b), in not showing "a second buried layer ... oriented in a second direction". Applicant respectfully disagrees and submits that figure 1(b) shows the deep trench capacitor 120 between the buried conductors 112 and 115, which are going into the page and are therefore shown and described as parallel in the specification at leats at the bottom of page 5. In light of the above, Applicant respectfully requests that the Examiner reconsider and withdrawn this rejection.

The Examiner states on page 6 that the specification does not provide support for claim 9, in not describing the first a second buried layers being parallel to the active layer. Applicant respectfully disagrees and submits that figure 1(b) shows the buried elements 112 and 114 going into the page and thus parallel to the active layer 118, and the specification on page 6, in the section discussing the embodiment of figure 1(b), states that there are additional levels of buried conductors, which level one of ordinary skill would understand to also be parallel to the first level and thus the active layer 118. Applicant respectfully requests that the Examiner reconsider and withdrawn this rejection.

Claim 12 and 20 have been cancelled herein without prejudice.

The Examiner states on page 6 that the specification does not provide support for claim 15 in not discussing that the second level of parallel conductive elements are located either in front of, or behind the deep trench capacitor. Applicant respectfully submits that one of ordinary skill in the art would understand from figure 1(b) and the discussion on page 6 regarding the additional level of buried elements that if the first level is going into the page, then the second level may be traversing the page from left to right and thus must be either in front of, or behind the deep trench capacitor. This is shown in other sections of the specification not related directly to the embodiment of figure 1(b), but still available to those of ordinary skill in the art. Further, the section of the specification related to all embodiments, in particular on page 8 and figure 3, show the two levels of buried interconnect. Applicant respectfully requests that the Examiner reconsider and withdrawn this rejection.

The Examiner states on page 6 that the specification does not provide support for claims 19 and 21 for not disclosing the different types of memory and the use of non-radioactive elements fro groups IVB, VB, VIB, VIIB and VIIIB. Applicant respectfully submits that the specification in the section related to all embodiments on page 14 discloses that the conductive elements, such as 112 and 114 of figure 1(b), may be formed from non-radioactive elements as found in the claims, and that page 6 line 4 discusses the use of multiple buried layers with regard to the embodiment of figure 1(b). Applicant respectfully requests that the Examiner reconsider and withdrawn this rejection.

§103 Rejection of the Claims

Claims 1-21 were rejected under 35 USC § 103(a) as being unpatentable over Okumura (U.S. Patent No. 4,912,535). Applicant respectfully traverses this rejection.

Applicant repeats the objection to the use of taking Official Notice of the missing elements of the single reference use in the Office Action, as discussed in the previous response. The cited reference of Okumura is admitted in the present outstanding Office Action to not disclose "a plurality of substantially buried conductive elements". The cited reference discloses a trench having "an impurity region formed on a side wall of the trench to be connected to the transistor and a conductor formed in the first trench to be in contact with the impurity region" (see col. 5, lines 5-10). Thus the cited reference is building the source/drains of the transistors in

the trenches 18 and 26, and making contact to the source/drain diffusions with polysilicon bit and word lines 1 and 9. The cited reference has the transistors being built in the substrate 3, and not in the active area, as recited in the present subject matter.

Applicant respectfully submits that the Examine in incorrect in stating on page 7 of the outstanding Office Action, that the Okamura reference "teaches in figures 6 and 7 and related text ... a dopes silicon substrate 3 having an active semiconductor layer 9 formed thereon; a conductive element 1 separated from the active semiconductor layer 9 by and surrounded by an oxide insulating material 24, 10b, 14", and submits that layer 9 in figures 6 and 7 is actually a polysilicon wordline (see col. 7, line 46) and not an active semiconductor layer as claimed; that the conductive element 1 is a polysilicon bit line; that layer 24 is the gate oxide of the transistor formed by diffusions 4 and 2 with the wordline 9 as the gate electrode and not an isolation oxide as claimed; that the poly bit line is not surrounded by the oxide insulating materials as claimed by the Examiner, but is in direct contact with the diffused source/drain region 2, as stated in the claims of Okamura and discussed at least at column 5, lines 1-10.

Further, Applicant respectfully submits that the cited reference, whether taken alone of in any combination with other well known art, fails to describe or suggest at least the combination of features of "*...a substrate having an active semiconductor layer formed thereon; a plurality of substantially parallel buried conductive elements separated from the active semiconductor layer by and surrounded by an insulating material;* ...", as recited in claim 1, and with similar language in the other independent claims. As noted above, the cited reference does not have an active semiconductor layer formed on a substrate. The substrate of the cited reference IS the active semiconductor layer. The cited reference does not have the conductive element buried or separated from the active semiconductor layer by an insulating material. In view of the above discussion, Applicant respectfully requests that this rejection be reconsidered and withdrawn.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney (612) 349-9587 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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Date 22 June '05

By _____
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I hereby certify that this paper is being transmitted by facsimile to the U.S. Patent and Trademark Office on the date shown below.

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